A Low-Offset High CMRR Current-Mode Instrumentation Amplifier Using Differential Difference Current Conveyor

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Abstract—Current-mode circuits are generally desirable for their high bandwidth. Moreover, current-mode instrumentation amplifiers have an advantage over voltage-mode counterparts that, they do not require precise resistor matching for a high CMRR. In this work, a current-mode instrumentation amplifier is proposed by employing Differential Difference Current Conveyor (DDCC). The proposed structure employs a single DDCC element, and an operational amplifier is used as a buffer or a final amplifier stage. After the explanation of the circuit, redundant output feedback (ROFB) circuit is presented to increase CMRR and to overcome the offset voltage at the output of the DDCC. The DDCC element is designed with 0.35μm technology and the proposed circuits are simulated using HSPICE. The proposed circuit with the feedback path provides more than 110 dB CMRR value at 1 MHz which is much higher than other current-mode implementations.

Keywords—current-mode circuits, instrumentation amplifier, DDCC, current-conveyor, CMRR.

I. INTRODUCTION

Instrumentation amplifiers are extensively used for engineering applications to amplify small differential signals. The key property of these amplifiers is the ability to reject undesired common mode voltages [1]. So that Common-Mode Rejection Ratio (CMRR) is the key parameter to measure the quality of an instrumentation amplifier. Generally, voltage-mode instrument amplifiers are employed in many of the engineering applications. Especially three opamp instrument amplifier is the most popular among the instrument amplifier topologies. [1-2]. However, in three opamp voltage-mode instrumentation amplifier, CMRR is directly dependent on resistor matching. Moreover, voltage-mode amplifiers are limited by gain-bandwidth product, i.e., as the gain increases, frequency band decreases. On the other hand, current-mode circuit bandwidth is not directly limited by gain [3]. One of the most popular implementations of Current-Mode Instrumentation Amplifier (CMIAs) [4] is depicted in Fig. 1. The output of the amplifier can be buffered by an operational amplifier to lower the output imbedance as well. The instrumentation amplifier shown in Fig. 1 employs two second generation current conveyors of plus type (CCII+). There are improvements over the basic CMIAs in [2, 5, 6-8].

In this work, Differential Difference Current Conveyor (DDCC) is employed for the implementation of the instrumentation amplifier. DDCC element is a rather new current conveyor topology compared to other implementations [7]. DDCC element working principle is based on difference operations of input voltages, so that it is easier to build an instrumentation amplifier. In this work, two current-mode instrumentation amplifier (CMIAs) circuits are proposed. The first proposed CMIAs is based on a single DDCC element, the circuit is very easy to implement and it has similar performance characteristics compared to the circuit depicted in Fig. 1. The second proposed circuit is based on redundant output feedback. In this circuit, another redundant DDCC component is employed to process the common-mode signals. Then, a negative feedback path is used to feed the redundant DDCC output back to both main and redundant DDCCs to increase the CMRR. The feedback input is also compensated using a RC filter at the feedback path to keep the circuit stable. The proposed circuit with redundant output feedback provides a very high CMRR up to high frequencies, compared to other CMIAs topologies.

Fig. 1. CCII+ based CMIA
II. DDCC BASED INSTRUMENTATION AMPLIFIER

DDCC is element is a three input two output current conveyor. The symbol of the DDCC element is depicted in Fig. 2(a). The output voltage $V_X$ is equal to the arithmetic operation as:

$$V_X = V_{Y1} - V_{Y2} + V_{Y3}.$$  

The node X current is copied to Z node as $I_X = I_Z$. The circuit equation of the idealized DDCC element in matrix form is as follows:

$$\begin{bmatrix}
V_X \\
I_{Y1} \\
I_{Y2} \\
I_{Y3} \\
I_Z
\end{bmatrix} = \begin{bmatrix}
1 & -1 & 1 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix} \begin{bmatrix}
V_{Y1} \\
V_{Y2} \\
V_{Y3} \\
I_X
\end{bmatrix}$$  \hspace{1cm} (1)

The detailed working principle of the DDCC element is explained in [7].

The DDCC element is very suitable for building an instrumentation amplifier. The proposed CMIA circuit is depicted in Fig. 2(b). Here, the gain is ideally achieved by $R_2/R_1$. To have a low impedance at the output, a voltage follower circuit is added as a buffer. The buffer stage can be replaced by an uninveter amplifier topology to have a finalized gain stage. However, the finalized gain stage should have low gain, since voltage-mode amplifiers suffer from gain-bandwidth product limitations. The voltage-mode stage is a single-ended amplifier and does not affect the CMRR value of the proposed amplifier.

The proposed circuit in Fig. 2(b) have similar performance characteristics with the conventional CMIA circuit shown in Fig. 1. The most important parameter of CMIA is the CMRR value, since the topology is used for differential small signal amplification. The proposed structure contains a single current conveyor and it is desirable for an easy implementation of a CMIA. The X node current is copied to Z node in the DDCC element as shown in Equation 1. However, there is a non-ideality for copying the current, which can be modeled as:

$$\begin{bmatrix}
V_X \\
I_{Y1} \\
I_{Y2} \\
I_{Y3} \\
I_Z
\end{bmatrix} = \begin{bmatrix}
1 & -1 & 1 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & \alpha
\end{bmatrix} \begin{bmatrix}
V_{Y1} \\
V_{Y2} \\
V_{Y3} \\
I_X
\end{bmatrix}$$  \hspace{1cm} (2)

The $\alpha$ value is generally between 0.9 and 1 in practice for the proposed circuit. Then the gain equation of the proposed CMIA is:

$$V_{out} = \alpha \frac{R_2}{R_1} (V_{in+} - V_{in-})$$  \hspace{1cm} (3)

The value of $\alpha$ can be extracted by SPICE simulations, or, it can be calculated by detailed circuit analysis. The DDCC element internal structure is depicted in Fig. 3, and the aspect ratios of the transistors are tabulated in Table 1. Here, it should be noted that the circuit in Fig. 3 with aspect ratios in Table 1 can be improved such as using cascoded stages for current mirrors. Here, the simplest architecture is employed for the analyses and simulations.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (µm/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1 - M_4$</td>
<td>10/1</td>
</tr>
<tr>
<td>$M_5, M_6$</td>
<td>15/1</td>
</tr>
<tr>
<td>$M_7 - M_{10}$</td>
<td>20/1</td>
</tr>
<tr>
<td>$M_{11}, M_{12}$</td>
<td>60/1</td>
</tr>
</tbody>
</table>

Fig. 3. Internal structure of DDCC element
In the proposed circuit the supply voltage is 3.3V, i.e. $V_{dd} = 3.3V$, and $V_{ss} = 0V$; $V_{bb}$ is 0.66V. The circuit is designed using 0.35µ AMS technology.

III. REDUNDANT OUTPUT FEEDBACK CIRCUIT

To increase the CMRR, a redundant output feedback (ROFB) circuit is developed for the proposed DDCC based instrumentation amplifier. By employing the proposed structure, CMRR of the circuit is boosted. The general diagram for the proposed structure is depicted in Fig. 4.

The working principle of the circuit in Fig. 4 is as follows. Using $R_{CM1}$ and $R_{CM2}$ resistors, the common mode voltage, i.e. $\frac{V_{in} + V_{in}}{2}$ is generated. The common-mode voltage is fed into the redundant DDCC in the diagram. Since the same voltage value is fed into the Y1 and Y2 nodes, the output should be zero according to (1), if Y3 voltage is zero. If there is an offset voltage available at Z node, using the negative feedback with gain = $K$, the Z node will be forced to be zero. Here, $K$ is selected to be 0.6. The Y3 voltage value that forces the redundant DDCC output Z to zero is also fed into the amplifier DDCC to remove any common-mode voltage and offset at the output. As a result, always the common-mode voltage is removed from the output. The aim of the redundant DDCC is that, if only common mode voltage is applied to the inputs the common-mode output of the circuit will be forced to zero. The feedback quantity is also fed into the main DDCC to have the same result, i.e., zeroing the common-mode output. There is a final gain stage at the output with a gain of G. The gain stage of the circuit is optional and can be built by an opamp in non-inverting amplifier topology. The gain of the final stage should be kept small (if large bandwidth is expected), because the voltage mode gain stage here has a limited gain-bandwidth product. The $R_{CM1}$ and $R_{CM2}$ resistance values should be selected to be high such as 1 Mega-ohms. These resistor mismatch for the $R_{CM1}$ and $R_{CM2}$ resistances is not critical for the CMRR of the circuit. If the input is needed to be isolated from the common-mode resistances, a voltage followers can be placed to the input nodes of the circuit. The buffers are represented as unity gain stages in Fig. 4, and can be built using opamp based voltage followers. Generally, a buffer stage is not required if the $R_{CM1}$ and $R_{CM2}$ resistance values are selected to be high.

For the ROFB circuit, there exists compensation stage built by a $R_{comp}$ and $C_{comp}$. These components are critical to keep away the circuit from oscillations. Gain and phase characteristics should be explored to have an appropriate $R$ and $C$ calculation for the compensation. The phase response from input to feedback output should remain in the margin of 90 degrees or less for stability. The detailed analysis for the selection of optimum feedback gain $K$ and calculations for $R_{comp}$ and $C_{comp}$ remains as future study.

![Fig. 4. General diagram for the proposed circuit with common-mode feedback path](image)

In the proposed circuit the supply voltage is 3.3V, i.e $V_{dd} = 3.3V$, and $V_{ss} = 0V$; $V_{bb}$ is 0.66V. The circuit is designed using 0.35µ AMS technology.

![Fig. 5. CMRR values of proposed CMIA: (a) without feedback; (b) with feedback](image)
IV. RESULTS

As shown in Fig. 5, the CMRR value greatly increases by employing ROFB circuit. The CMRR is measured to be 135 dB for the proposed CMIA with feedback. The CMRR of the proposed circuit with feedback is much higher than the works in [3], [5] and [8] especially at high frequencies. The comparison for the proposed circuit with other works is given in Table II. The actual circuit diagram of the proposed CMIA is shown in Fig. 6. The gain of the circuit depicted in Fig. 6 can be calculated as:

\[ V_{out} = \alpha \frac{R_2}{R_1} (1 + \frac{R_4}{R_3}) (V_{in+} - V_{in-}) \]  

(4)

The \( \alpha \) value is extracted from HSPICE simulations and here \( \alpha \approx 0.9 \) for the DDCC in Fig. 3 is used. Internal structure of the DDCC can be optimized to reach idealized values. For the HSPICE simulations, the resistor values are selected to be \( R_1 = 1k \), \( R_2 = 20k \), \( R_3 = 1k \) and \( R_4 = 5k \). The opamp in the feedback path acts as an inverting amplifier with gain of \( K = 0.6 \) which is provided by the ratios of \( R_3/R_2 \), i.e., \( 12k/20k = 0.6 \). The positive terminal of the opamp of the feedback path is connected to ground to virtually connect the redundant DDCC’s Z terminal resistor to ground. Various K values and its effect in CMRR is left as future study. The final stage gain is kept relatively small, since the voltage-mode amplifier suffers from gain-bandwidth product. The resulting gain of the circuit is measured to be approximately 100. The Proposed circuit -3dB point resides at 10 MHz. The CMRR value at 1MHz is 112 dB and it is 88 dB at 10 MHz. It should be noted that, the feedback circuit does not limit the bandwidth of the circuit, since it only regulates the common-mode error signal. However, the feedback circuit greatly improves the CMRR.

V. CONCLUSION

In this work, a current-mode instrumentation amplifier is proposed using DDCC element. Moreover, by applying a novel redundant output feedback (ROFB) technique to the amplifier, common-mode signals minimized resulting with an exceptional CMRR value even at high frequencies compared to other CMIA topologies. The proposed circuit has higher CMRR value with simple structure compared to previous implementations. The mismatch analysis of the transistors and IC implementation remains as future work.

REFERENCES