A High Gain and Low-Offset Current-Mode Instrumentation Amplifier Using Differential Difference Current Conveyors

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Abstract—In this work, a current-mode high CMRR and low offset instrumentation amplifier is proposed. In the structure, only differential difference current conveyors (DDCC) are employed. The offset of the instrumentation amplifier is suppressed using an integrator feedback stage. The CMRR of the system is simulated using mismatch models for the DDCC elements employed. The CMRR of the instrumentation amplifier is independent of resistor mismatches, and, high CMRR is achieved if good matching of the differential transistors of each current conveyor is provided. The proposed instrumentation amplifier is designed using 0.35µm technology and simulated using HSPICE. The designed instrumentation amplifier provides high CMRR with low offset and it is especially suitable for AC coupled measurements. The simplicity of the design structure is the main advantage of the provided design where only DDCC elements are required for high CMRR and high output swing.

Keywords—current-mode circuits, low offset instrumentation amplifier, DDCC, current-conveyor, CMRR.

I. INTRODUCTION

Instrumentation amplifiers are extensively used for engineering applications to amplify small differential signals. The key property of these amplifiers is the ability to reject undesired common mode voltages [1]. Therefore, Common-Mode Rejection Ratio (CMRR) is the key parameter to measure the quality of an instrumentation amplifier. Generally, voltage-mode instrument amplifiers are employed in many of the engineering applications. Especially three opamp instrument amplifier is the most popular structure among instrument amplifier topologies. [1-2]. A major drawback of the three opamp voltage-mode instrumentation amplifier is that its CMRR is directly dependent on resistor matching. Moreover, voltage-mode amplifiers are limited by gain-bandwidth product, i.e., as the gain increases, frequency band-width decreases. An alternative is to use current-mode circuits where bandwidth is not directly limited by gain [3, 10-11]. One of the most popular implementations of Current-Mode Instrumentation Amplifier (CMIA) [4] is depicted in Fig. 1. The gain formula of the CMIA shown in Fig. 1 is:

\[ V_{\text{out}} = \frac{R_1}{R_2} (V_{a+} - V_{a-}) \]  

Improvements over the basic CMIA can be found in [2, 5, 6-8]. In many of the CMIA papers, variety of the amplifier topologies are simulated and high CMRR values are reported. However, generally mismatch models for the transistors of the current conveyors are not included in the simulations. In this work, random variations are also included in the differential input stages, which is the main source of limited CMRR in differential amplifiers [9].

In this work, an alternative CMIA is proposed using differential difference current conveyors (DDCC). DDCC element is a three-input two-output current conveyor that provides algebraic operations of the input transferred to the output. The algebraic operations of the Y1, Y2 and Y3 inputs are equal to the X output. Then, the current of X output is copied to the Z node. Variety of gain stages can be built using DDCC elements because of rich algebraic input operands. The circuit equation of the idealized DDCC element in matrix form is as follows:

\[ \begin{bmatrix}
V_X \\
I_{Y1} \\
I_{Y2} \\
I_{Y3} \\
I_Z
\end{bmatrix} = 
\begin{bmatrix}
1 & -1 & 1 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3 \\
I_X
\end{bmatrix} \]  

Fig. 1. CCII+ based CMIA
In this paper, various amplifier topologies are presented using DDCC elements. Then, a high CMRR and low output offset current-mode instrumentation amplifier is proposed. Also, an improved internal structure of a DDCC stage is developed which provides specifications close to ideal DDCC element. The main specifications of the DDCC presented are very low input impedance at node X, high impedance at node Z, and precise current copying characteristics from node X to node Z. Also the structure provides near rail-to-rail output swing which is generally important for instrumentation amplifiers.

II. DDCC BASED CMIA TOPOLOGIES

Two of the amplifier topologies developed using DDCC elements are depicted in Fig. 2. (a) and (b), respectively. The amplifier topology in Fig. 2. (a) has similar properties with the CMIA shown in Fig 1. with higher gain. The voltage generated at node X of the first and second DDCCs are:

\[ V_{X1} = V_{in+} - V_{in-} + V_{in+} \]  
\[ V_{X2} = V_{in+} - V_{in-} + V_{in-} \]

respectively. The currents of the X nodes of the DDCCs are:

\[ I_{x1} = -I_{x2} = \frac{V_{X1} - V_{X2}}{R_2} = \frac{3}{R_2} (V_{in+} - V_{in-}) \]

Since \( I_{x1} = I_{Z1}, I_{x2} = I_{Z2} \),

\[ V_{OUT+} = V_{Z1} = I_{Z1} R_2 = \frac{3}{R_2} (V_{in+} - V_{in-}) \]
\[ V_{OUT-} = V_{Z2} = I_{Z2} R_1 = -\frac{3}{R_2} (V_{in+} - V_{in-}) \]

The second amplifier shown in Fig. 2 (b) employs only a single current conveyor. The topology exhibits lower CMRR whenever transistor mismatch exists in the differential inputs in the internal structure, which is the case that occurs inevitably. The gain equation of the circuit shown in Fig. 2 (b) is simply:

\[ V_{OUT} = \frac{R_1}{R_2} (V_{in+} - V_{in-}) \]

A high gain and high CMRR instrumentation amplifier is designed using two of the differential amplifiers given in in Fig.2 (a) and (b). The proposed CMIA is shown in Fig. 3. The proposed instrumentation amplifier is based on three basic stages: Pre-amplifier, amplifier and current-mode integrator based offset cancellation loop. Here, the pre-amplifier stage has relatively low gain. The pre-amplifier stage removes the common-mode signals and differential outputs without common-mode signals appears at the outputs of the pre-
amplifier. The second stage is a simple differential amplifier which subtracts the two differential outputs of the pre-amplifier stage. The gain of the proposed CMIA is calculated using (6), (7) and (8) as:

$$ V_{OUT} = 6 \frac{R_1}{R_2} \frac{R_3}{R_4} (V_{m+} - V_{m-}) $$  \hspace{1cm} (9) 

Although the common-mode input voltage is suppressed, there may still exist an offset voltage which may cause saturation at the output stage. To remove the remaining offset voltage, an integrator based feedback stage is included in the second amplifier stage. The integrator works as a low-pass filter, and integrates the output voltage and subtracts the accumulated offset voltage from the input. The feedback loop is composed of current-mode integrator circuit that feeds the integrated offset voltage to the input of the amplifier state. If the integrator stage is employed in the amplifier, only AC signals are amplified, DC signals and low frequency signals are filtered out. The integrator function is calculated as:

$$ V_{FB} = - \frac{1}{R_F C_F} \int V_{OUTX} dt $$  \hspace{1cm} (10) 

Here, $V_{OUTX}$ is the X port output of the second stage DDCC. The negative sign of the integrator is available since the feedback is made through Y2 port of the DDCC which has negative coefficient as shown in (2). The integrator feedback results as a high-pass filter, so that $R_F$ and $C_F$ should be kept as high as possible, not to filter out low frequency signal components. If DC signals should be amplified as well, the Y3 input of the amplifier should be grounded, then the integrator loop is deactivated.

The internal structure of the DDCC element used in the CMIA is shown in Fig. 4. Each of the bias currents are selected as 10µA in the internal structure. To make the output stage rail-to-rail, a low voltage cascode current mirror is used at port Z of the DDCC element. The internal structure of the current sources are also built using low-voltage cascode style. The supply voltage is given as ±1.65 V, and the voltage swing at the output is ±1.55 V. For the simulations, the selected component values are as follows: $R_1 = 10kΩ$, $R_2 = 2kΩ$, $R_3 = 50kΩ$, $R_4 = 1.5kΩ$ are selected, resulting with a gain of 1000. Also, $R_F$ and $C_F$ are selected as 100kΩ and 2µF, respectively. Transistor aspect ratios of the DDCC element is shown in Table I.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L (µm/µm)</th>
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<tbody>
<tr>
<td>M1 - M4</td>
<td>40/4</td>
</tr>
<tr>
<td>M5, M6, M7</td>
<td>40/1</td>
</tr>
<tr>
<td>M8, M9</td>
<td>20/1</td>
</tr>
<tr>
<td>M10, M11</td>
<td>50/1</td>
</tr>
<tr>
<td>M12, M13, M14, M15</td>
<td>120/1</td>
</tr>
<tr>
<td>M16, M17</td>
<td>50/0.7</td>
</tr>
</tbody>
</table>

III. SIMULATION RESULTS

The proposed structure provides high gain together with high CMRR. Moreover, using the integrator loop as feedback, a low offset is provided which makes the proposed CMIA an efficient differential amplifier for variety of applications. Class AB output stage with emitter followers provide low X resistance and Z node with low voltage cascode provides high swing with accurate output both of which improve design accuracy.

As the main concern is high CMRR in most of the high gain instrumentation amplifiers, a detailed analysis is required. In many of the research papers on instrumentation amplifiers, mismatch analysis of the transistors is not mentioned. Although current-mode instrumentation amplifiers are not affected by resistor mismatch, their CMRR is limited by transistor mismatch in the matched pairs. So that, in most of the applications requiring high CMRR, main concern should be matching of each differential pair in any differential path on
each amplifier. In this work, a random mismatch is applied for each of the differential pairs at each current conveyor during simulations. With perfect matching conditions, high CMRR is recorded for various CMIA topologies. The proposed structure is simulated under mismatch conditions, and there is still high CMRR is recorded. The simulation results for the CMRR of the proposed structure is shown in Fig. 5.

The AC analysis of the amplifier is shown in Fig. 6. The bandwidth of the CMIA is 1.75 MHz for the gain of 1000 using given component values. The proposed CMIA provides wide bandwidth according to the gain and current consumption values. The proposed structure has 67 µV input referred offset voltage. The bandwidth of the proposed CMIA is 1.75 MHz. The CMRR and bandwidth of the design is compared to other applications is shown in Table II. Design summary is given in Table III.

IV. CONCLUSION

In this work, a current-mode instrumentation amplifier is proposed using only DDCC elements. The structure is based on two stage cascaded current-mode differential amplifiers with integrator feedback to minimize offset voltage. The structure has superior CMRR values and two stage cascaded gain stage provides an easy adjustment for high gain as well. Amplification from multiple paths at the input stage improves noise performance and CMRR related to differential pair mismatches. The proposed simple and efficient and suitable for general purpose differential amplification where high gain and bandwidth together with low offset is desired. The output of the circuit provides nearly rail-to-rail output. The bandwidth of the amplifier is 1.75 MHz and the CMRR is 125 dB according to the simulation results. For the simulations, mismatch models of the differential pairs are also included, which is one of the bottlenecks when designing for high CMRR and low output offset voltage.

TABLE II. CMRR RECORDINGS OF VARIOUS CMIAS.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>CMRR (dB) @ 10kHz</th>
<th>Bandwidth</th>
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<tbody>
<tr>
<td>[4]</td>
<td>80</td>
<td>10 kHz</td>
</tr>
<tr>
<td>[2]</td>
<td>120</td>
<td>20 kHz</td>
</tr>
<tr>
<td>[8]</td>
<td>95</td>
<td>80 kHz</td>
</tr>
<tr>
<td>[12]</td>
<td>112</td>
<td>10 kHz</td>
</tr>
<tr>
<td>This work (Fig. 3)</td>
<td>125</td>
<td>1.75 MHz</td>
</tr>
</tbody>
</table>

REFERENCES